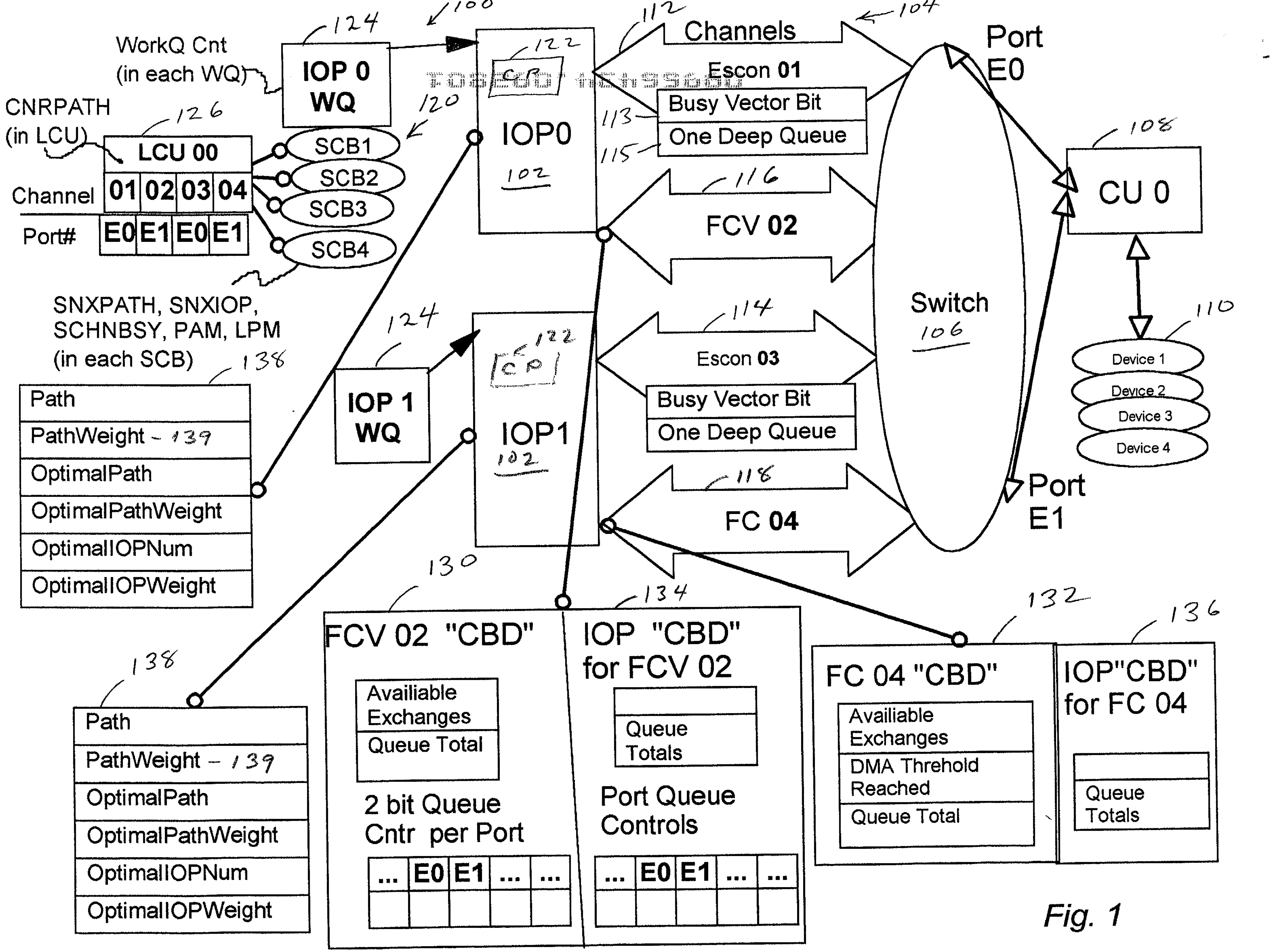
100
104
112
Channels
Escon 01
Busy Vector Bit
One Deep Queue
113
115
FCV 02
116
Escon 03
114
Busy Vector Bit
One Deep Queue
FC 04
118
Switch
106
Port
E0
Port
E1
CU 0
108
Device 1
Device 2
Device 3
Device 4
110
IOP0
102
122
CP
IOP1
102
IOP 0
WQ
124
IOP 1
WQ
WorkQ Cnt
(in each WQ)
CNRPATH
(in LCU)
126
LCU 00
Channel
01 02 03 04
Port#
E0 E1 E0 E1
SCB1
SCB2
SCB3
SCB4
120
SNXPATH, SNXIOP,
SCHNBSY, PAM, LPM
(in each SCB)
138
Path
PathWeight - 139
OptimalPath
OptimalPathWeight
OptimalIOPNum
OptimalIOPWeight
130
FCV 02 "CBD"
Availiable
Exchanges
Queue Total
2 bit Queue
Cntr per Port
... E0 E1 ... ...
134
IOP "CBD"
for FCV 02
Queue
Totals
Port Queue
Controls
... E0 E1 ... ...
132
FC 04 "CBD"
Availiable
Exchanges
DMA Threhold
Reached
Queue Total
136
IOP"CBD"
for FC 04
Queue
Totals

Fig. 1

130

Word Offset	Bit	Description	Initial Setting by IOP	Value stored by CHN
0	0-7	Sequence Number	0	Sequence #
	8-15	Available Exchanges	0	Available LCs
	16-31	Total Queued in Channel	0	Total Queued
1 (IOP will set for zSeries only! Zero, Otherwise)	0-7	Control Block Code	0xFC	0xFC
	8	Control Block Code Qualifier	0	0
	9-12	Reserved	0	0
	13	CHN unavailable (NOT USED)	0	0
	14	CHN Allowed to Store into Area	1	1
	15	CHN did Store into Area	0	**1**
	16-23	CHID	CHID	CHID
	24-31	Reserved	0	0
2-17	2x256	2 bits per Port Queue Counters	0	Set per Port
18-31		reserved - for either CHN or IOP (just in case)	0	**Don't Store Anything**

Fig. 2

132

Word Offset	Bit	Description	Initial Setting by IOP	Value stored by CHN
0	0-7	Sequence Number	0	Sequence #
	8-15	Available Exchanges	0	Available Exch.
	16-31	Total Queued in Channel	0	Total Queued
1 (IOP will set for zSeries only! Zero, Other-wise)	0-7	Control Block Code	0xFC	0xFC
	8	Control Block Code Qualifier	0	0
	9-12	Reserved	0	0
	13	CHN unavailable (NOT USED)	0	0
	14	CHN Allowed to Store into Area	1	1
	15	CHN did Store into Area	0	**1**
	16-23	CHID	CHID	CHID
	24	DMA Storage Request Queue Threshold Reached	0	Set to 1 if reached
	25-31	Reserved	0	0
2-31		reserved - for either CHN or IOP (just in case)	0	**Don't Store Anything**

Fig. 3

134

Word Offset	Bit	Description	Initial Setting by IOP	Value stored by IOP
0	0-7	Sequence Number	0	Sequence #
	8-15	Reserved	0	0
	16-31	Total Queued in Channel	0	Total Queued
1 (IOP will set for zSeries only! Zero, Other-wise)	0-7	Control Block Code	0xFC	0xFC
	8	reserved	1	1
	9-13		0	0
	14	IOP Allowed to store into Area	1	1
	15	IOP did Store into Area	0	**1**
	16-23	CHID	CHID	CHID
	24-31	Reserved	0	0
2-9	1x256	IOP_Q2Busy	0	Set per Port
10-17	1x256	IOP_Q1Busy	0	Set per Port
18-25	1x256	IOP_PrevQBusy	0	Set per Port
26-31		Reserved	0	0

Fig. 4

136

Word Offset	Bit	Description	Initial Setting by IOP	Value stored by IOP
0	0-7	Sequence Number	0	Sequence #
	8-15	Reserved	0	0
	16-31	Total Queued in Channel	0	Total Queued
1 (IOP will set for zSeries only! Zero, Other-wise)	0-7	Control Block Code	0xFC	0xFC
	8	Control Block Code Qualifier	1	1
	9-13	Reserved	0	0
	14	IOP Allowed to store into Area	1	1
	15	IOP did Store into Area	0	1
	16-23	CHID	CHID	CHID
	24-31	Reserved	0	0
2-31		Reserved	0	0

Fig. 5

139

Bit	Description	FCV	FC	non-Ficon
0-1	Number of Starts Queued to Port -OR- Busyness of Channel	CHN_Qcount(port) + IOP_Q1busy(port) + IOP_Q2busy(port) (Total number of Starts queued to the port)	0	0
2			FC__MaxStoreReqs + "**AEX**" *Note: To compute* **AEX**: If AvailableExchanges = 0, then "**AEX**" = 1. Otherwise, "**AEX**" = 0	One Deep Queue Bit from Vector. For Pre-zSeries, set bit to 0
3				Channel Busy Vector Bit
4	Link Init Req'd	If Link Init required, set bit to 1		
5	Previously Queued Start	IOP_PrevQbusy(port)	0	0
6	Destination Port Busy	~~FCV_DPbusy(port)~~ 0	0	0
7	Channel Hardware Availablity	If AvailableExchanges = 0, set bit to 1. Otherwise, set to 0	"**AEX**" -OR'd with - FC__MaxStoreReqs	Channel Busy Vector Bit
8-13	Reserved	0	0	0
14	Unknown PathWeight State	If FICON path not storing statistics in HSA (FC/FCV_StatsActive = 0), set this bit to 1. For Pre-zSeries non-FICON paths: If path is on another IOP -OR- the Channel Busy Vector is on, set this bit to 1		
15	Favor Preferred Path	Set to 1 if Preferred Path bit is ON & this path is NOT preferred path		
16-31	Total Queued in Channel	FCV_TotalQueued + IOP_TotalQueued	FC__TotalQueued + IOP_TotalQueued	Channel Busy Vector Bit x 8

Fig. 6